

Autumn Examinations, 2003

Exam Code(s) 3BP121

Exam(s) Third Year Electronic and Computer Engineering

Module Code(s) EE321

Module(s) Analogue Systems Design II

Paper No. 2

Repeat Paper Yes Special Paper _____

External Examiner(s) Professor S. McLaughlin

Internal Examiner(s) Professor D.J. Wilcox

Dr. J. Breslin

Instructions:

Answer 3 questions.

All questions carry equal marks.

Duration 2hrs

No. of Answer books 1

Requirements:

Handout _____

MCQ _____

Statistical Tables _____

Graph Paper _____

Log Graph Paper _____

Other Material Yes Standard Mathematics Tables

No. of Pages 4

Department(s) Electronic Engineering

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NATIONAL UNIVERSITY OF IRELAND, GALWAY

AUTUMN EXAMINATIONS 2003

THIRD YEAR ELECTRONIC AND COMPUTER ENGINEERING

EE321 ANALOGUE SYSTEMS DESIGN II

Professor S. McLaughlin
Professor D.J. Wilcox
Dr. J. Breslin

Duration of Examination: **TWO** hours
Instructions: Answer **THREE** questions

1.

(a)

Write a short description for each of the following types of diode [3 x 3 marks].

- Schottky diode
- Varactor diode
- LED

(b)

A Zener diode circuit for voltage regulation is given in Fig. 1.

- (i) Sketch the i_D vs. v_D characteristic for a Zener diode showing the various regions of operation [2 marks].
- (ii) In which region does the Zener diode operate for the voltage regulator application shown [1 mark]?
- (iii) For varying source voltage and load current, analyse the circuit in Fig. 1 to determine the proper range of values for R_i that will allow the diode to maintain a constant output voltage (by keeping the Zener current between its minimum and maximum values) [6 marks].
- (iv) Define percentage regulation for the Zener diode voltage regulator [2 marks].

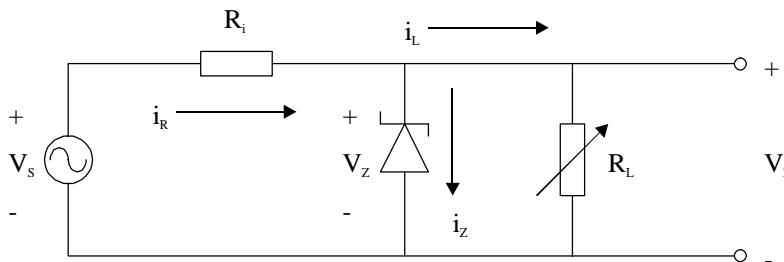


Fig. 1

[cont'd]

2.

(a)

- (i) Describe the properties of an *ideal diode* [2 marks].
- (ii) What is the name of the circuit in Fig. 2 (a), and what is its purpose [1 mark]?
- (iii) For a sinusoidal input V_S with a peak-to-peak voltage of 5 V, sketch the output V_O if the characteristic curve of the real diode is as shown in Fig. 2 (b) [4 marks].

(b)

- (i) Describe the effect on V_O of placing a capacitor C between points A and B in the circuit shown in Fig. 2 (a), i.e. in parallel with the load [4 marks].
- (ii) Give an expression for the percentage ripple on the output signal V_O when the capacitor is included in the circuit [4 marks].
- (iii) Calculate the percentage ripple if the circuit parameters are as follows: the period of the input sinusoidal waveform is 16.7 ms, the input peak-to-peak voltage is 5 V, the load resistance is 100 Ω , and the capacitor value is 1000 μF . What would happen if the capacitor value C was increased [5 marks]?

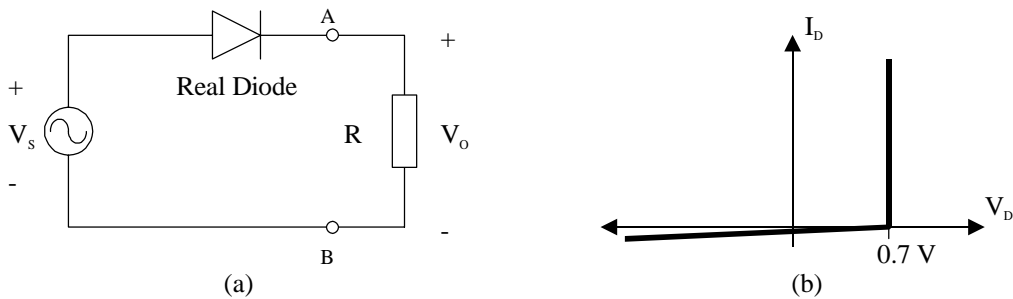


Fig. 2

3.

- (a) Perform a DC analysis of the base biasing section of the common emitter amplifier as shown in Fig. 3, and hence derive formulæ for the position of the DC operating point on the characteristic curves [8 marks].
- (b) Explain why it is important for small signal voltage amplification to set the quiescent point in the BJT's linear mode of operation using the DC bias circuit [4 marks].
- (c) What is the effect of the bypass capacitor C_E in this circuit [1 mark]?
- (d) Draw a small signal model for the common emitter amplifier circuit in Fig. 3, and using this model derive an expression for the gain of the amplifier [7 marks].

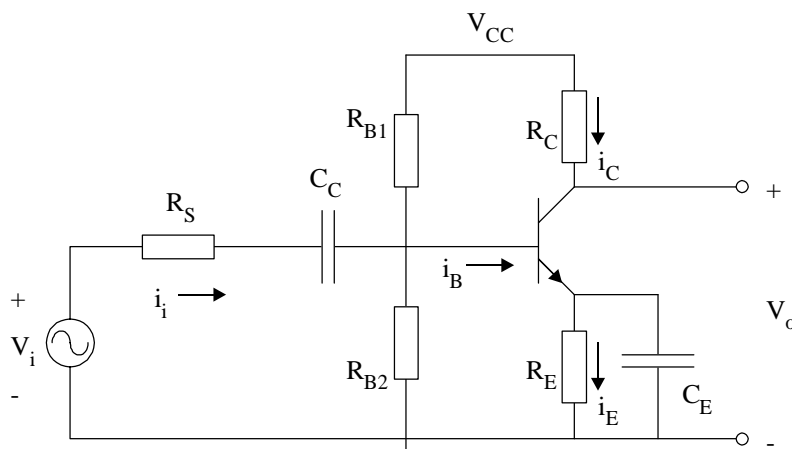


Fig. 3

[cont'd]

4.

- (a) Illustrate the operating modes of the n-channel JFET device using cross sectional diagrams [6 marks].
- (b) Calculate the DC operating point of the JFET amplifier shown in Fig. 4, where $I_{DSS} = 8 \text{ mA}$ and $V_{DSPO} = 6 \text{ V}$ [9 marks].

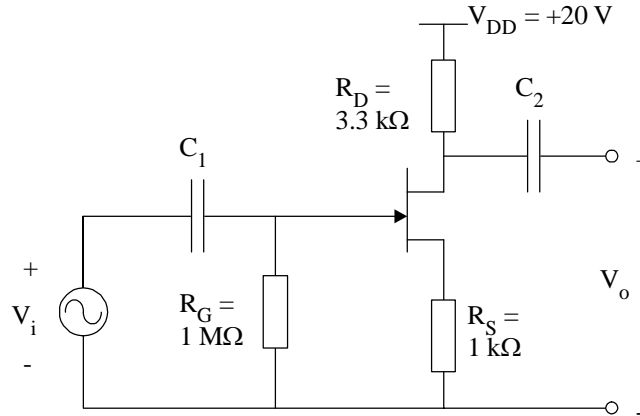


Fig. 4

- (c) Illustrate with a cross-section a D-MOSFET and explain how the conducting channel can be “enhanced” by a correctly applied gate voltage [5 marks].

5.

- (a) Explain the operation of an integrator using the following points in your explanation:
- Circuit diagram [3 marks].
 - Derive an expression for v_o [6 marks].
 - Sketch the v_o you would expect for a square wave input (your diagram should include both input and output waveforms) [4 marks].
- (b) Explain briefly what is meant by the following specifications in practical operational amplifier circuits (suggest typical values where appropriate):
- Input offset voltage [2 marks].
 - Slew rate [2 marks].
- (c) Calculate the input offset voltage for the circuit in Fig. 5 given $V_o = -8 \text{ V}$ [3 marks].

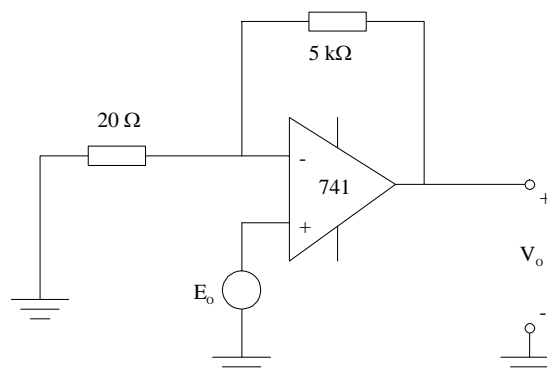


Fig. 5