

Semester I Examinations, 2003/2004

Exam Code(s) 2BN121
 2BP121

Exam(s) Second Year Electronic Engineering
 Second Year Electronic and Computer Engineering

Module Code(s) EE207

Module(s) Digital Systems I

Paper No. _____
Repeat Paper _____ Special Paper _____

External Examiner(s) Professor S. McLaughlin
Internal Examiner(s) Professor D.J. Wilcox
 Dr. J. Breslin

Instructions: Answer 3 questions.
 All questions carry equal marks.

Duration 2hrs
No. of Answer books 1

Requirements:
Handout _____
MCQ _____
Statistical Tables _____
Graph Paper _____
Log Graph Paper _____
Other Material _____

No. of Pages 4
Department(s) Electronic Engineering

1. *Digital Computers and Information*

- (a) Multiply the following two numbers in binary using the shift and add algorithm: $13_{10} \times 6_{10}$.
[4 marks]
- (b) Add the following two numbers in BCD: $448_{10} + 489_{10}$.
[4 marks]
- (c) The ASCII hexadecimal code for a left square bracket “[” is $5B_{16}$. Convert this code to binary, and explain how even and odd parity coding would be used to detect errors in the transmission of this code.
[6 marks]
- (d) Using two bits, explain the advantage of using gray code over straight binary.
[6 marks]

2. *Combinational Logic Circuits*

- (a) Prove that $\overline{xy\bar{z}} + \overline{xy\bar{z}} + xy\bar{z} = \overline{xz} + y\bar{z}$ (note that $\overline{\bar{x}} \equiv x'$).
[2 marks]
- (b) Simplify the function $F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 7, 14, 15)$ on a Karnaugh map using the prime implicants method.
[4 marks]
- (c) Simplify the function $g(a, b, c, d)$ whose Karnaugh map is shown in Figure 1.

	cd			
ab	00	01	11	10
	0	1	0	1
01	1	1	0	1
11	0	0	x	x
10	1	1	x	x

Figure 1

- [2 marks]
- (d) Define the *propagation delay* characteristic for digital logic families, and illustrate the propagation delay for a typical inverter. What is the benefit of using the *inertial delay* method as opposed to the *transport delay* method in digital logic?
[6 marks]
- (e) Show how the basic NAND, NOR and NOT gates would be implemented using *fully complementary* CMOS networks.
[6 marks]

[cont'd]

3. *Combinational Logic Design*

- (a) Design a code converter circuit that converts a BCD codeword to its corresponding Excess-3 codeword, showing derived truth tables and Karnaugh maps. [11 marks]
- (b) For the wind direction detector as shown in Figure 2, design a simple encoder to convert the eight wind directions in unary code to 3-bit binary code. What are the ambiguities with such an encoder?

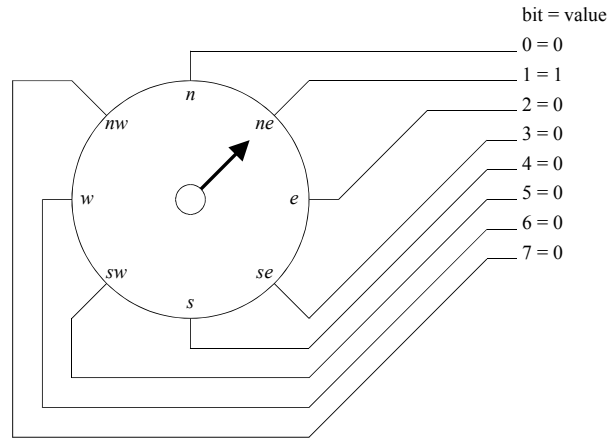


Figure 2

[9 marks]

4. *Sequential Logic Circuits*

- (a) What is the difference between synchronous and asynchronous machines? [3 marks]
- (b) Draw the logic diagram and function table for an SR latch with a clock signal. [3 marks]
- (c) Describe both Mealy and Moore machine models using diagrams where necessary. [8 marks]
- (d) Recreate the state table from the state diagram for a Mealy model type system in Figure 3.

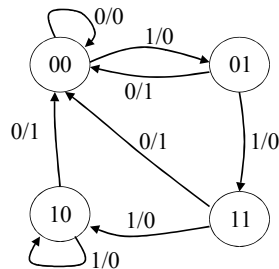


Figure 3

[6 marks]

[cont'd]

5. *Registers / Counters / PLDs*

(a) What is the difference between a register and a counter? [2 marks]

(b) Design and draw a 4-bit D-type shift register and a 4-bit JK-type (upwards) ripple counter. [4 marks]

(c) Explain each of the following terms: PLD, ROM, PLA and PAL. [8 marks]

(d) Show how the combinational circuit described by the following equations would be implemented on the PAL as shown in Figure 4 (note that $\overline{A} \equiv A'$):

$$W = \overline{ABC} + CD$$

$$X = \overline{ABC} + \overline{ACD} + A\overline{CD} + BCD$$

$$Y = \overline{ACD} + ACD + \overline{ABD}$$

You should reproduce the completed Figure 4 in your answer book.

[6 marks]

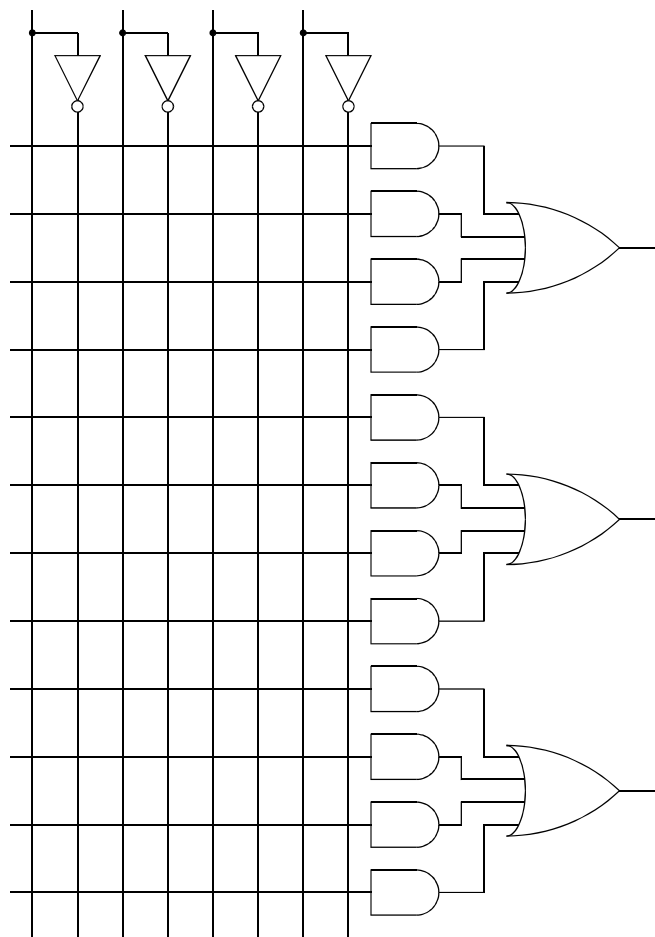


Figure 4