

Autumn Examinations, 2004

Exam Code(s)	<u>2BN121</u> <u>2BP121</u>
Exam(s)	<u>Second Year Electronic Engineering</u> <u>Second Year Electronic and Computer Engineering</u>
Module Code(s)	<u>EE207</u>
Module(s)	<u>Digital Systems I</u>
Paper No.	_____
Repeat Paper	<u>Yes</u> Special Paper _____
External Examiner(s)	<u>Professor S. McLaughlin</u>
Internal Examiner(s)	<u>Professor D.J. Wilcox</u> <u>Dr. J. Breslin</u>

Instructions:

Answer 3 questions.
All questions carry equal marks.

Duration	<u>2hrs</u>
No. of Answer books	<u>1</u>

Requirements:

Handout	_____
MCQ	_____
Statistical Tables	_____
Graph Paper	_____
Log Graph Paper	_____
Other Material	_____

No. of Pages	<u>4</u>
Department(s)	<u>Electronic Engineering</u>

1. *Digital Computers and Information*

- (a) Multiply the following two numbers in binary using the shift and add algorithm: $13_{10} \times 6_{10}$.
[4 marks]
- (b) Convert 365_{10} to both binary and BCD.
[4 marks]
- (c) The ASCII hexadecimal code for a left square bracket “[” is $5B_{16}$. Convert this code to binary, and explain how even and odd parity coding would be used to detect errors in the transmission of this code.
[6 marks]
- (d) Using two bits, explain the advantage of using gray code over straight binary.
[6 marks]

2. *Combinational Logic Circuits*

- (a) Find $G(x, y, z)$, the complement of $F(x, y, z) = x\bar{y}z + \bar{x}yz$ (note that $\bar{\bar{x}} = x$).
[2 marks]
- (b) Simplify the function $F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 7, 14, 15)$ on a Karnaugh map using the prime implicants method.
[4 marks]
- (c) Simplify the function $g(a, b, c, d)$ whose Karnaugh map is shown in Figure 1.

		cd			
	ab	00	01	11	10
		x	1	0	0
	01	1	x	0	x
	11	1	x	x	1
	10	0	x	x	0

Figure 1

- (d) Define each of the following terms for digital logic families: *fan out*, *fan in*, *noise margin*, and *power dissipation*.
[4 x 1½ marks]
- (e) What is a CMOS transmission gate? Show how an XOR gate could be implemented using transmission gates.
[6 marks]

[cont'd]

3. *Combinational Logic Design*

- (a) Derive the truth table for a code converter circuit that converts a BCD codeword to its corresponding digit on a seven-segment display. [7 marks]

- (b) For the wind direction detector in Figure 2, design a simple encoder to convert the eight directions in unary code to 3-bit binary code. What are the ambiguities with this encoder?

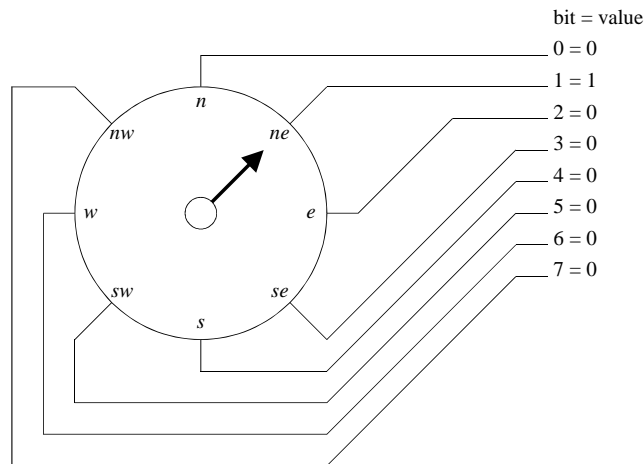


Figure 2

[9 marks]

- (c) Show how a full adder with $S = \sum m(1, 2, 4, 7)$ and $C = \sum m(3, 5, 6, 7)$ could be implemented using a 3-to-8 decoder. [4 marks]

[4 marks]

4. *Sequential Logic Circuits*

- (a) What is the difference between synchronous and asynchronous machines? [3 marks]

[3 marks]

- (b) Draw the logic diagram and function table for an SR latch with a clock signal. [3 marks]

[3 marks]

- (c) Describe both Mealy and Moore machine models using diagrams where necessary. [8 marks]

[8 marks]

- (d) Recreate the state table from the state diagram for a Mealy model type system in Figure 3.

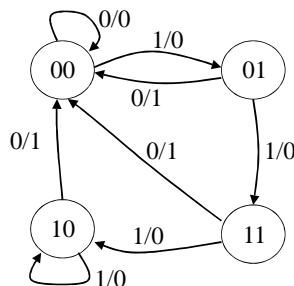


Figure 3

[6 marks]

[cont'd]

5. Registers / Counters / PLDs

- (a) What is the difference between a register and a counter? [2 marks]
- (b) Design and draw a 4-bit D-type shift register and a 4-bit JK-type (upwards) ripple counter. [4 marks]
- (c) Explain each of the following terms: PLD, ROM, PLA and PAL. [8 marks]
- (d) Show how the combinational circuit described by the following equations would be implemented on the PAL as shown in Figure 4 (note that $\overline{A} \equiv A'$):

$$W = \overline{A}BC + CD$$

$$X = \overline{A}BC + \overline{A}CD + ACD + BCD$$

$$Y = \overline{A}CD + ACD + \overline{A}BD$$

You should reproduce the completed Figure 4 in your answer book.

[6 marks]

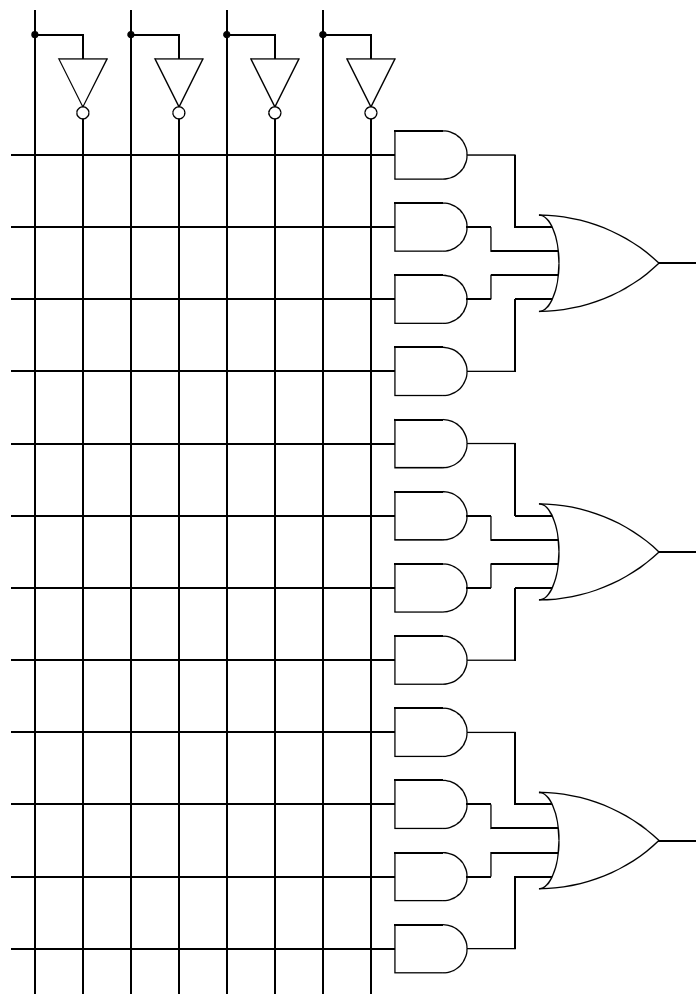


Figure 4